IN THE CLAIMS:

A full listing of the pending claims of this application, including any amendments made by this paper, follows below:

1. (Currently Amended) A method for forming a sensor comprising the steps of:

providing a base wafer;

forming a sensor cavity in said base wafer;

after said forming step, coupling a diaphragm wafer to said base wafer, said diaphragm wafer including a diaphragm portion, a sacrificial portion, and an insulating layer disposed between said diaphragm portion and said sacrificial portion, and wherein said diaphragm wafer is coupled to said base wafer such said diaphragm portion generally covers said sensor cavity;

reducing ~~the~~ a thickness of said diaphragm wafer by removing at least part of said sacrificial portion while using said insulating layer as an etch stop; and

forming or locating at least one piezo resistive portion on said diaphragm portion.

2. (Previously Presented) The method of claim 1 wherein said diaphragm wafer is a silicon-on-insulator wafer including upper and lower silicon layers separated by said insulating layer, and wherein said upper silicon layer includes said sacrificial portion and said lower silicon layer includes said diaphragm portion, and wherein said reducing step includes removing substantially all of said upper silicon layer of said diaphragm wafer located over said sensor cavity.

3. (Previously Presented) The method of claim 1 wherein said coupling step includes coupling said diaphragm wafer to said base wafer by fusion silicon bonding.

4. (Previously Presented) The method of claim 1 further comprising the step of reducing the thickness of said base wafer.

5. (Previously Presented) The method of claim 4 wherein said base wafer is a silicon-on-insulator wafer including upper and lower silicon layers separated by an insulating layer, and wherein said reducing step of said base wafer includes removing said lower silicon layer of said base wafer.

6. (Previously Presented) The method of claim 1 wherein said base wafer and said diaphragm wafer are both silicon-on-insulator wafers.

7. (Previously Presented) The method of claim 1 wherein said forming or locating step includes bombarding at least a portion of said diaphragm wafer with high energy atoms using implantation methods.

8. (Previously Presented) The method of claim 1 further comprising the step of depositing at least two conductive leads on said diaphragm wafer, said leads being electrically coupled to said at least one piezo resistive portion.

9. (Currently Amended) The method of claim 8 further comprising the step of etching at least two grooves in said base wafer to form a surface for receiving an external wire therein, and wherein depositing step includes depositing said leads such that at least part of each lead is located in ~~said trough~~ one of said grooves.

10. (Currently Amended) The method of claim 1 wherein said sensor cavity is generally circular in a top view.

11. (Currently Amended) The method of claim 1 wherein said ~~first~~ sensor cavity forming step includes etching said sensor cavity using deep reactive ion etching.

12. (Previously Presented) The method of claim 1 further comprising the step of coupling a carrier wafer to said diaphragm wafer, etching a dicing lane around said sensor to release said sensor from said base wafer and diaphragm wafer, and removing said carrier wafer.

13. (Previously Presented) The method of claim 12 wherein said coupling step including bonding said carrier wafer to said diaphragm wafer, said etching step including etching using deep reactive ion etching.

14. (Previously Presented) The method of claim 12 wherein said sensor includes a body portion including said diaphragm portion and said at least one piezo resistive portion, and wherein said sensor includes a frame extending around said body portion, and wherein said carrier wafer is coupled to said frame and not coupled to said body portion during said coupling step.

15. (Previously Presented) The method of claim 12 further comprising the step of, before said coupling step, depositing a layer of conductive material on said diaphragm wafer to form at least two leads electrically coupled to said piezo resistive portion, and wherein at least part of said conductive material forms a spacer located adjacent an end of said sensor, and wherein said carrier wafer is located on top of said spacer during said coupling step.

16. (Previously Presented) The method of claim 1 further comprising the steps of etching a dicing lane in said diaphragm wafer and said base wafer to define a body portion having said sensor located thereon, a frame located around said body portion, and an arm extending between said frame and said body portion.

17. (Previously Presented) The method of claim 16 further comprising the step of separating said sensor from said diaphragm wafer by breaking arm to separate the body portion from said frame.

18. (Previously Presented) The method of claim 16 wherein said etching includes deep reactive ion etching.

19. (Currently Amended) The method of claim 1 wherein said ~~first~~ sensor cavity forming step includes etching said sensor cavity and etching a trough in said base wafer using deep reactive ion etching, and wherein the method further includes the step of depositing or growing an insulating layer on said base wafer after said first forming step.

20. (Previously Presented) The method of claim 19 wherein said base wafer and said diaphragm wafers are both silicon-on-insulator wafers including upper and lower silicon layers separated by an insulating layer, and wherein the method further includes the step of removing said upper silicon layer and said insulating layer of said diaphragm wafer, and bombarding selected portions of said lower silicon layer of said diaphragm wafer with high energy atoms to form said at least one piezo resistive portion.

21. (Previously Presented) The method of claim 20 further comprising the steps of depositing a passivation layer on said diaphragm wafer, etching said passivation layer to expose at least part of said at least one piezo resistive portion, and depositing a conductive material on said diaphragm wafer such that at least part of said conductive material contacts said exposed part of said at least one piezo resistive portion.

22. (Previously Presented) The method of claim 21 further comprising the step of removing any portions of said diaphragm wafer located over said trough, and forming at least two grooves in said trough.

23. (Previously Presented) The method of claim 22 further comprising the step of depositing an auxiliary passivation layer on said diaphragm wafer coating said conductive material, etching said auxiliary passivation layer to at least partially expose said conductive material, and depositing an auxiliary layer of conductive material on said sensor such that said auxiliary layer of conductive material contacts said conductive material, and such that at least part of said auxiliary layer of conductive material is located in each of said grooves.

24. (Previously Presented) The method of claim 1 wherein said diaphragm wafer is coupled to said base wafer such that said sensor cavity is sealed between and located between said diaphragm portion and said base wafer.

25. (Currently Amended) A method for forming a sensor comprising the steps of:

providing a base wafer;

etching a sensor cavity in said base wafer;

providing a silicon-on-insulator diaphragm wafer including upper and lower silicon layers separated by an insulating layer;

coupling said diaphragm wafer to said base wafer such that a diaphragm portion of said ~~base~~ diaphragm wafer is located over said sensor cavity;

etching said base wafer to reduce ~~the~~ a thickness of said base wafer;

removing at least said upper silicon layer of said diaphragm wafer to reduce ~~the~~ a thickness of said ~~base wafer and form a~~ diaphragm portion; and

depositing at least one piezo resistor on said diaphragm portion.

26. (Currently Amended) A method for forming a sensor comprising the steps of:

providing a base wafer;

forming a sensor cavity in said base wafer;

coupling a diaphragm wafer to said base wafer such that a diaphragm portion of said diaphragm wafer is located over said sensor cavity;

reducing ~~the~~ a thickness of said base wafer; and

forming or locating at least one piezo resistive portion on said diaphragm portion, wherein said base wafer includes an upper layer, a lower layer, and an insulating layer disposed between said upper layer and said lower layer, and wherein said reducing step includes removing said lower layer of said base wafer while using said insulating layer as an etch stop.

27. (Currently Amended) A method for forming a sensor comprising the steps of:

providing a silicon base wafer;

forming a sensor cavity in said base wafer;

coupling a silicon diaphragm wafer to said base wafer by fusion silicon bonding, said diaphragm wafer including a diaphragm portion, at least one of said base wafer or said diaphragm wafer being a silicon-on-insulator wafer having an upper silicon layer, a lower silicon layer and an insulating layer disposed therebetween, and wherein said diaphragm wafer is coupled to said base wafer such that said diaphragm portion generally covers said sensor cavity; and

forming or locating at least one piezo resistive portion on said diaphragm portion.

28-65. (Canceled)

66. (Currently Amended) The method of claim ~~65~~ 26 wherein said base wafer is a silicon-on-insulator wafer, said upper and lower portions are silicon, and wherein said insulating layer is an oxide.

67. (Previously Presented) The method of claim 27 further comprising the step of reducing the thickness of said silicon-on-insulator wafer by removing one of said upper or lower layers while using said insulating layer as an etch stop.

68. (Currently Amended) A method for forming a sensor comprising the steps of:

providing a base wafer which is a semiconductor-on-insulator wafer;

forming a sensor cavity in said base wafer;

coupling a diaphragm wafer to said base wafer, said diaphragm wafer being a semiconductor-on-insulator wafer and including a diaphragm semiconductor portion, a sacrificial semiconductor portion, and an insulating layer disposed between said diaphragm portion and said sacrificial portion, and wherein said diaphragm wafer is coupled to said base wafer such said diaphragm portion generally covers said sensor cavity;

reducing ~~the~~ a thickness of said diaphragm wafer by removing at least part of said sacrificial portion while using said insulating layer as an etch stop; and

forming or locating at least one piezo resistive portion on said diaphragm portion.

69. (Previously Presented) The method of claim 68 wherein each of said semiconductor-on-insulator wafers includes an upper semiconductor layer, a lower semiconductor layer and an insulating layer located between said upper and lower semiconductor layers.

70. (Previously Presented) The method of claim 69 wherein both of said semiconductor-on-insulator wafers are silicon-on-insulator wafers.